

**CLAIMS:**

- 1 1. A receiver comprising:  
2 an oscillator outputting phases of a clock signal; and  
3 a retiming mechanism coupled to said oscillator having circuitry for receiving  
4 said phases of said clock signal, circuitry for receiving serial data, and circuitry  
5 operable to reduce timing uncertainties in said serial data by outputting a value of said  
6 serial data sampled at a particular phase of said clock.
- 1 2. The receiver as recited in claim 1, wherein said retiming mechanism  
2 comprises a plurality of first units, wherein each of said plurality of first units  
3 comprises circuitry for sampling said serial data using a particular phase of said  
4 clock.
- 1 3. The receiver as recited in claim 2, wherein each of said plurality of first units  
2 comprises circuitry for receiving said particular phase of said clock and a complement  
3 of said particular phase of said clock and said serial data.
- 1 4. The receiver as recited in claim 2, wherein said retiming mechanism further  
2 comprises a plurality of second units, wherein each of said plurality of second units is  
3 associated with a particular first unit, wherein each of said plurality of second units  
4 comprises circuitry for outputting a value of said serial data sampled by said  
5 associated first unit upon activation.
- 1 5. The receiver as recited in claim 4, wherein a particular second unit of said  
2 plurality of second units is activated based on a logical state of each input to said  
3 particular second unit.

- 1        6.        The receiver as recited in claim 5, wherein said logical state of each input is  
2        determined based on combinational logic using said phases of said clock and  
3        complements of said phases of said clock.

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1 7. A system comprising:  
2 a transmission medium;  
3 a transmitter coupled to said transmission medium configured to convert  
4 parallel data to a serial form; and  
5 a receiver coupled to said transmission medium, where said receiver  
6 comprises:  
7 an oscillator outputting phases of a clock signal; and  
8 a retiming mechanism coupled to said oscillator having circuitry for  
9 receiving said phases of said clock signal, circuitry for receiving serial data, and  
10 circuitry operable to reduce timing uncertainties in said serial data by outputting a  
11 value of said serial data sampled at a particular phase of said clock.

1 8. The system as recited in claim 7, wherein said retiming mechanism comprises  
2 a plurality of first units, wherein each of said plurality of first units comprises  
3 circuitry for sampling said serial data using a particular phase of said clock.

1 9. The system as recited in claim 8, wherein each of said plurality of first units  
2 comprises circuitry for receiving said particular phase of said clock and a complement  
3 of said particular phase of said clock and said serial data.

1 10. The system as recited in claim 8, wherein said retiming mechanism further  
2 comprises a plurality of second units, wherein each of said plurality of second units is  
3 associated with a particular first unit, wherein each of said plurality of second units  
4 comprises circuitry for outputting a value of said serial data sampled by said  
5 associated first unit upon activation.

1 11. The system as recited in claim 10, wherein a particular second unit of said  
2 plurality of second units is activated based on a logical state of each input to said  
3 particular second unit.

1 12. The system as recited in claim 11, wherein said logical state of each input is  
2 determined based on combinational logic using said phases of said clock and  
3 complements of said phases of said clock.